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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,217	02/19/2004	Kevin Nolish	P63993-USA	5328

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EXAMINER	
MEHRMANESH, ELMIRA	

ART UNIT	PAPER NUMBER
2113	

MAIL DATE	DELIVERY MODE
12/10/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/782,217	NOLISH ET AL.	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-7 and 10-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7 and 10-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to an amendment filed on August 6, 2009 for the application of Nolish et al., for a "Method, apparatus and software for preventing switch failures in the presence of faults" filed February 19, 2004.

Claims 1, 4-7, and 10-19 are pending in the application.

Claims 2-3 and 8-9 have been cancelled.

Claims 1, 4-7, and 10-19 have been amended.

Claims 1, 4-7, and 10-19 are rejected under 35 USC § 102.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4-7, and 10-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Goodrum et al. (U.S. Patent No. 5,822,512).

As per claim 1, Goodrum discloses a switch for transferring data comprising:

at least one master unit (Fig. 3, elements 101, 123) a plurality of slave units (Fig. 3, elements 103, 121); a bus through which the master unit communicates with the slave units (Fig. 3, element 24); and

a detecting mechanism for detecting whether a slave unit is a failed slave unit, wherein if the slave unit is a failed slave unit, causing the switch to abnormally terminate (col. 89, lines 12-20); and

memory in the switch comprising a software program that, upon abnormal termination of the switch, directs the at least one master unit to avoid further accessing a failed slave unit of the plurality of slave units by storing status information relating to the failed slave unit, in persistent storage, that survives across the abnormal termination of the switch (col. 89, lines 54-67 through col. 90, lines 1-14) and thereafter preventing the master unit from attempting to access the failed slave unit (col. 90, lines 14-20).

As per claim 4, Goodrum discloses the software program causes the master unit to automatically recover when the detecting mechanism causes the master unit to abnormally terminate (col. 89, lines 20-45).

As per claim 5, Goodrum discloses detecting mechanism includes a hardware watchdog device (col. 88, lines 51-54).

As per claim 6, Goodrum discloses a method for transferring data comprising the steps of:

attempting to access a slave unit (col. 90, lines 1-8) of a plurality of slave units (Fig. 3, elements 103, 121) of a switch by a master unit (Fig. 3, elements 101, 123) of

the switch with a signal through a bus through which the master unit and the slave unit communicate (Fig. 3, element 24); and

detecting whether the slave unit is a failed slave unit, wherein if said slave unit is a failed slave unit, causing the switch to abnormally terminate (col. 89, lines 12-20); and

responsive to abnormal termination of the switch, automatically recovering the switch from the failed slave unit (col. 89, lines 12-20) with a software program in the switch that directs the master unit to avoid further accessing the failed slave unit of the plurality of slave units by storing status information relating to the failed slave unit in persistent storage that survives across abnormal termination of the switch (col. 89, lines 54-67 through col. 90, lines 1-14) and thereafter preventing the master unit from attempting to access the failed slave unit (col. 90, lines 14-20).

As per claim 7, Goodrum discloses the recovering step includes the step of obtaining status information about the slave units from persistent storage (Fig. 39A, elements 408, 422).

As per claim 10, Goodrum discloses changing information in persistent storage associated with the first slave unit from identified as failed to identified as good if the master unit does not terminate abnormally after the master unit attempts to contact the slave unit (Fig. 39B, elements 420, 424, 426).

As per claim 11, Goodrum discloses the step of setting a variable slot chosen from amongst a plurality of slots of the switch not marked as potentially bad (Fig. 39B, element, 426).

As per claim 12, Goodrum discloses the step of determining whether the first slave unit is physically present in a first slot of the plurality of slots (Fig. 39B, element, 426).

As per claim 13, Goodrum discloses the step of determining the first slot is marked to be skipped (Fig. 39A, element, 422).

As per claim 14, Goodrum discloses the step of marking the variable slot as potentially bad if it is not marked potentially bad (Fig. 39B, element, 440) and (col. 90, lines 49-52).

As per claim 15, Goodrum discloses the step of reporting the variable slot as containing broken hardware and preventing the master unit from attempting to access the variable slot if the variable slot is marked to be skipped (Fig. 39A, element, 422).

As per claim 16, Goodrum discloses the step of attempting to access hardware present in the variable slot if the variable slot is marked potentially bad (Fig. 39A-B).

As per claim 17, Goodrum discloses the step of marking the variable slot as good if the switch did not abnormally terminate when the master unit accessed the first slave unit (Fig. 39B, element, 426).

As per claim 18, Goodrum discloses the step of enabling normal operations on hardware present in the variable slot if the variable slot is marked as good (Fig. 39A, element, 412).

As per claim 19, Goodrum discloses the step of setting the variable slot to a next slot of the plurality of slots (Fig. 39B, element, 420).

Response to Arguments

Applicant's arguments filed August 6, 2009 have been fully considered but they are not persuasive.

As per claims 1 and 6 in response to applicant's arguments that Goodrum fails to teach the claimed limitation "a software program in the switch that directs the master unit to avoid further accessing the failed slave unit of the plurality of slave units", the Examiner respectfully disagrees and would like to point out to col. 89 lines 54-57, wherein Goodrum discloses "Referring to FIG. 39, **the BIOS isolation handler first logs 408 to the fail status information portion of the NVRAM** the bus history and bus state vector information stored in the history and vector FIFOs in the bus monitor

127. The bus history and bus state vector FIFOs are read and their contents transferred to the NVRAM."

Note col. 90, lines 8-20, wherein Goordum further discloses isolating the faulty device based on the failed status information stored in the persistent storage:

"If the routine determines 414 that the bus-hang pending bit is set active, **the slot is indicated as being failed (e.g., by setting active a fail flag for that slot) in the fail status information portion of the NVRAM**. Next, the loop consisting of steps 412, 414, 416, 418 and 420 is performed until all populated slots have been checked.

If all populated slots have been checked 416, **the routine checks 424 to determine if any slot is indicated as failed in the fail status information portion of the NVRAM. If so, the routine 398 re-enables 426 only the non-failing slots.** Then, the isolation-in-progress EV is cleared 428, and the BIOS isolation routine is complete."

Thus storing the failed status information (*fail flag*) in persistent storage (*NVRAM*) and isolating said failed device as disclosed by Goodrum, reads on the claimed limitation as recited in claim 1 and 6.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1 .136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1 .136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Robert W. Beausoliel, Jr./
Supervisory Patent Examiner, Art Unit 2113